PRELIMINARY

Analog Signal Input Stereo Class D Power Amplifier

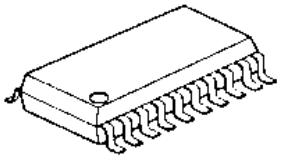
■ GENERAL DESCRIPTION

The **NJU8755** is an analog signal input stereo class D power amplifier. The **NJU8755** includes Inversion operatinal amplifier input circuit, PWM modulators, an output-short protector and a low voltage detector. The **NJU8755** is configured as a BTL amplifier capable of delivering up to 1.2W/channel with simple external LC low-pass filters. A BTL configuration eliminates the need for external AC coupling capacitors.

Class-D achieves high output-efficiency, which leads to long battery life for battery powered applications, thus the **NJU8755** is ideally suited for portable audio, note-PC, etc.

■ PACKAGE OUTLINE

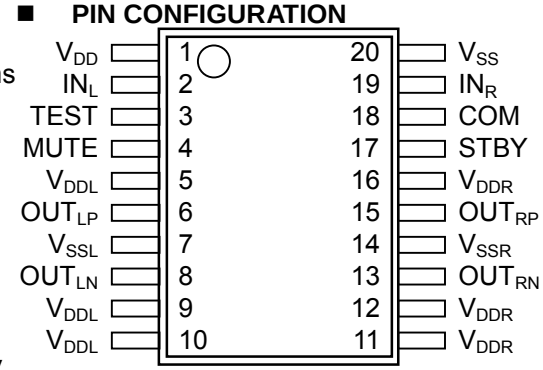
NJU8755V



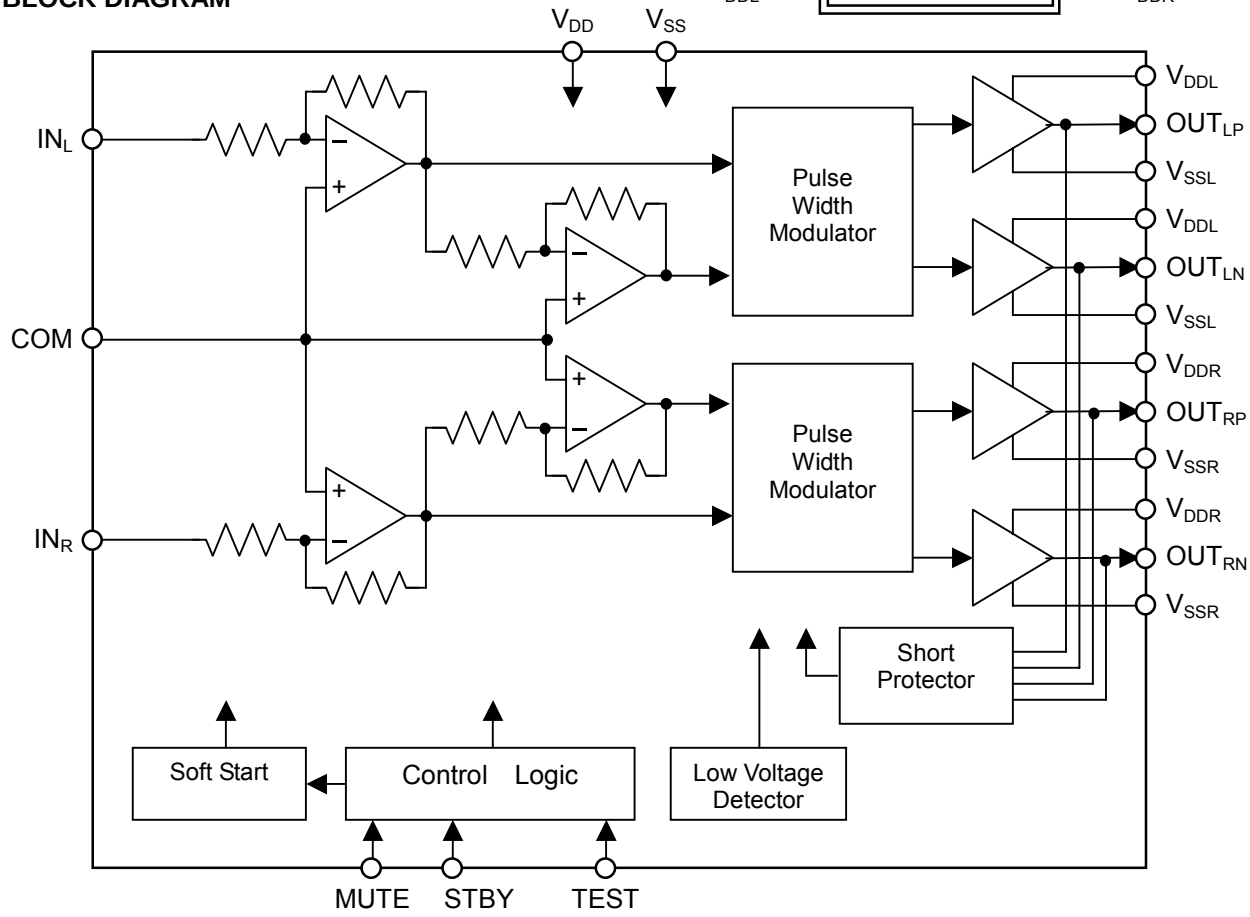
■ FEATURES

- 2-Channel Analog Signal Input
- 2-Channel BTL Outputs :1.2W/channel at 5V into 8Ohms
- Standby(Hi-Z), BPZ Control
- Built-in Short Protector
- Built-in Low Voltage Detector
- Operating Voltage 2.7 ~ 5.25V
- CMOS Technology
- Package Outline SSOP20

■ PIN CONFIGURATION



■ BLOCK DIAGRAM



■ **PIN DESCRIPTION**

No.	SYMBOL	I/O	FUNCTION
1	V_{DD}	–	Power supply : V_{DD}=5.0V
2	IN_L	I	L-channel signal input
3	TEST	I	Maker test This pin must be connected to GND.
4	MUTE	I	Mute control L : Mute ON H : Mute OFF
5 9 10	V_{DDL}	–	L-channel power supply : V_{DDL}=5.0V
6	OUT_{LP}	O	L-channel positive output
7	V_{SSL}	–	L-channel power GND
8	OUT_{LN}	O	L-channel negative output
11 12 16	V_{DDR}	–	R-channel power supply : V_{DDL}=5.0V
13	OUT_{RN}	O	R-channel negative output
14	V_{SSR}	–	R-channel power GND : V_{SSL}=0V
15	OUT_{RP}	O	R-channel positive output
17	STBY	I	Standby control L : Standby ON H : Standby OFF
18	COM	I	Analog common
19	IN_R	I	R-channel signal input
20	V_{SS}	–	Power GND : V_{SS}=0V

*The relations of "V_{SS}= V_{SSL}= V_{SSR}=0V" and "V_{DD}= V_{DDL}=V_{DDR}" must be maintained.
*Pin No.4(MUTE) and 17(STBY) must be connected to V_{DD}, when these pins are not used.

■ FUNCTIONAL DESCRIPTION

(1) Signal Output

The $OUT_{LP/LN}$ and $OUT_{RP/RN}$ generate respectively L-channel and R-channel PMW output signals, which will be converted to analog signal via external 2nd-order or higher LC filter. A switching regulator with a high response against a voltage fluctuation is the best selection for the V_{DDL} and V_{DDR}, which are the power supply for output drivers. To obtain better T.H.D. performance, the stabilization of the power is key.

(2) Standby

By setting the STBY pin to "L", the standby mode is enabled. In the standby mode, the entire functions of the **NJU8755** enter a low-power state, and the output pins($OUT_{LP/LN}$ and $OUT_{RP/RN}$) are in high impedance.

(3) Mute

By setting the MUTE pin to "L", the Mute function is enabled, and the output pins($OUT_{LP/LN}$ and $OUT_{RP/RN}$) output square wave(Duty: 50%).

(4) Low Voltage Detector

When the power supply voltage drops down to below V_{DD}(MIN), the internal oscillation is halted not to generate unwanted frequency, and the output pins($OUT_{LP/LN}$ and $OUT_{RP/RN}$) become in high impedance.

(5) Short Protection Circuit

The short protector, which protects the **NJU8755** from high short-circuit current, turns off the output drivers of L-channel and R-channel independently. After about 5 seconds from the protection, the **NJU8755** returns to normal operation. The short protector is enabled in response to following accidents.

Short between OUT_{LP} and OUT_{LN}
Short between OUT_{LP} and V_{SSL}
Short between OUT_{LN} and V_{SSL}
Short between OUT_{RP} and OUT_{RN}
Short between OUT_{RP} and V_{SSR}
Short between OUT_{RN} and V_{SSR}

Note 1) The detectable current and the period for the protection depend on the power supply voltage and ambient temperature.

Note 2) The short protector is not effective for a long term short-circuit but for an instantaneous accident. Continuous high-current may cause permanent damage to **NJU8755**.

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	-0.3 ~ +5.5	V
	V_{DDL}	-0.3 ~ +5.5	V
	V_{DDR}	-0.3 ~ +5.5	V
Input Voltage	Vin	-0.3 ~ V_{DD}+0.3	V
Operating Temperature	Topr	-40 ~ +85	°C
Storage Temperature	Tstg	-40 ~ +125	°C
Power Dissipation	P_D	300 (SSOP20)	mW

Note 1) All voltage are relative to "V_{SS}= V_{SSL}= V_{SSR}=0V" reference.

Note 2) The LSI must be used inside of the "Absolute maximum ratings". Otherwise, a stress may cause permanent damage to the LSI.

Note 3) De-coupling capacitors for V_{DD}-$V_{SS,}$ V_{DDL}-V_{SSL} , and V_{DDR}-V_{SSR} should be connected for stable operation.

Note 4) Power Dissipation

The class-D amplifiers are more power efficient, and dissipate less than general analog-amplifiers. In theory, the **NJU8755** can deliver quite high output-power such as 1.2W/channel at =5V into 8ohms, and total power is supposed to be 2.4W. For this reason, it looks as if the **NJU8755** exceeds the absolute maximum rating of the power dissipation. However, in practice, the effective output-power of usual music sound is only about 1/10 of its maximum output power, thus it may never exceed the absolute maximum rating.

The maximum power dissipation in the system is calculated, as shown below.

$Pdmax(W) = (Tjmax(°C) - Ta(°C)) / \theta ja$

Pdmax: Maximum Power Dissipation, Tjmax: Junction Temperature = 125°C
Ta: Ambient Temperature, θja: Thermal Resistance of package(SSOP20) = 333°C/W

Power dissipation of the **NJU8755** itself is calculated, as shown below.

$Pd(W) = P_O(W) \times R_O(\Omega) / R_L(\Omega) + Pd_{IC}(W)$

Pd: Power Dissipation, P_O: Output Power, $R_{O:}$ Internal Resistance(output driver)
R_L: Load Resistance, $Pd_{IC:}$ Power of internal circuit

■ ELECTRICAL CHARACTERISTICS

(Ta=25°C, V_{DD}= V_{DDL}= V_{DDR}=5.0V, V_{SS}=V_{SSL}=V_{SSR}=0V, Input Signal=1kHz, Input Signal Level=200mVrms, Frequency Band=20Hz~20kHz, Load Impedance=8Ω, 2nd-order 34kHz LC Filter(Q=0.75))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	Note
V_{DD},V_{DDP},V_{DDN} Supply Voltage	V_{DD}		2.7	5.0	5.25	V	
Input Impedance	Z_{IN}	IN_L, IN_R pins	-	20	-	kΩ	
Voltage Gain	A_V		-	23	-	dB	
Output Power Efficiency	Eeff	Output THD=10%	80	-	-	%	4
Output THD	THD	Po=0.6W	-	-	0.1	%	
Output Power	Po	Output THD=10%	-	1.2	-	W/ch	
S/N	SN	A weight	TBD	TBD	-	dB	
Dynamic Range	Drange	A weight	TBD	TBD	-	dB	
Channel Separation	Echn	EIAJ(1kHz)	60	-	-	dB	
Output Level Difference Between L- and R- channels	CHD		-	-	3	dB	
Maximum Mute Attenuation	MAT		90	-	-	dB	
Operating Current (Standby)	I_{ST}		-	-	10	μA	
Operating Current (No signal input)	I_{DD}	No Filter No Load	-	-	10	mA	
Input Voltage	V_{IH}	MUTE, STBY pins	$0.7V_{DD}$	-	V_{DD}	V	
	V_{IL}	MUTE, STBY pins	0	-	$0.3V_{DD}$	V	
Input Leakage Current	I_{LK}	MUTE, STBY pins	-	-	±1.0	μA	

Note 5) Test system of the output THD, S/N and Dynamic Range
The output THD, S/N and dynamic range are tested in the system shown in Figure1, where a 2nd-order LC LPF and another filter incorporated in an audio analyzer are used.

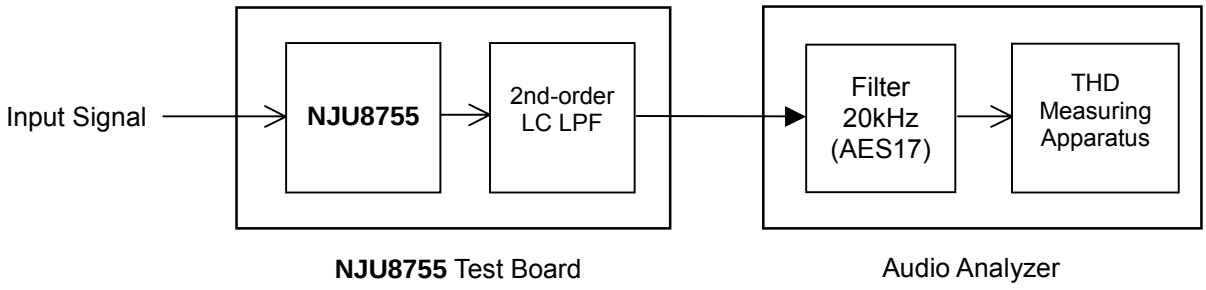


Figure 1. Output THD, S/N and Dynamic Range Test System

2nd-order LPF : fc=34kHz / Refer to “Typical Application Circuit”.
Filters : 22Hz HPF + 20kHz LPF(AES17)
(with the A-Weight filter for S/N and Dynamic-range tests)

■ TYPICAL APPLICATION CIRCUIT

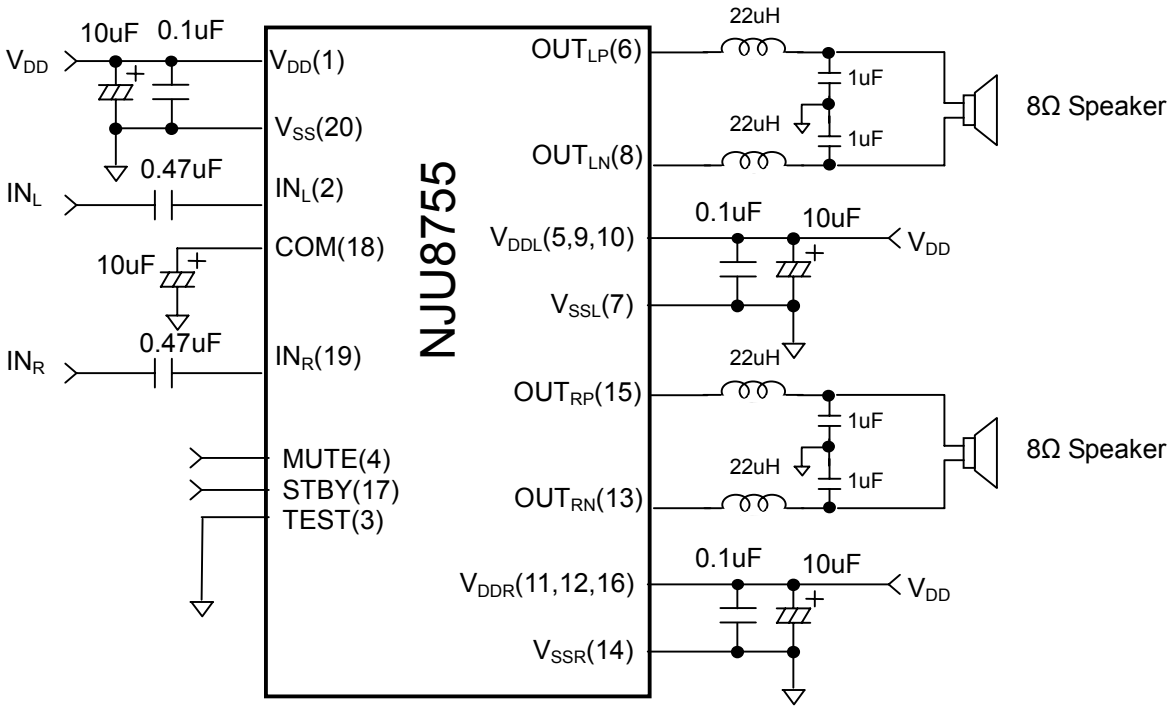


Figure 2. Application Circuit example

Note 6) De-coupling capacitors must be connected between each power supply pin and GND.
Note 7) A switching regulator with a high response against a voltage fluctuation is ideal for the V_{DDL} and V_{DDR} to obtain better THD performance.
Note 8) Testing actual samples in your system is highly recommended. The typical application circuit is one of examples.
Note 9) The transition time for MUTE and STBY signals must be less than 100us. Otherwise, a malfunction might occur.
Note10) (1) – (20) indicates pin number.